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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/302, 21/3065, 21/308, 21/76, 23/13 — A1

(11) International Publication Number: WO 97/27621

(43) International Publication Date: 31 July 1997 (31.07.97)

(21) International Application Number: PCT/US97/00991

(22) International Filing Date: 23 January 1997 (23.01.97)

(30) Priority Data:
08/592,785 26 January 1996 (26.01.96) US

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(81) Designated States: CN, CZ, HU, JP, KR, NO, PL, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SELECTIVE-ETCH EDGE TRIMMING PROCESS FOR MANUFACTURING SEMICONDUCTOR-ON-INSULATOR WAFERS

(57) Abstract

The peripheral edge of a semiconductor-on-insulator wafer is trimmed by forming a preferentially etchable masking layer over all but the edge margin of the surface of the semiconductor layer and selectively etching the semiconductor layer, preferably without etching either the masking layer or the insulating layer. The thickness, thickness variation, surface roughness and surface defects of the semiconductor layer approximate, before edge-trimming, the same characteristics of a wafer in its final, finished form which is suitable for device fabrication. As applied to bonded semiconductor-on-insulator wafers, the process removes lamination defects located between the semiconductor layer and the insulating layer. The edge-trimmed semiconductor-on-insulator wafer resulting from the method of the present invention is characterized by a semiconductor layer having a sharp peripheral edge. Bonded semiconductor-on-insulator wafers are further characterized by a lack of peripheral lamination defects.

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SELECTIVE-ETCH EDGE TRIMMING PROCESS FOR MANUFACTURING SEMICONDUCTOR-ON-INSULATOR WAFERS

BACKGROUND OF THE INVENTION

The present invention generally relates to the manufacture of semiconductor-on-insulator wafers, and specifically, to a process for trimming the peripheral edge of such wafers. The invention also relates to semiconductor-on-insulator wafers having an edge-trimmed semiconductor layer.

Semiconductor-on-insulator (SOI) wafers typically comprise, in succession, a handle or substrate layer, an insulating layer, and a semiconductor layer. Such wafers are manufactured by several techniques known in the art, including primarily implanted oxygen (SIMOX) methods and direct bonding methods. Japanese Kokoku Patent No. 62-34716 discloses another method involving localized growth of the semiconductor layer from a single crystal projection extended through the oxide layer.

The peripheral edges of semiconductor-on-insulator wafers are trimmed to make them cosmetically acceptable and functionally compatible with subsequent integrated circuit fabrication steps. Edge trimming is particularly important for bonded semiconductor-on-insulator wafers that have lamination defects near their peripheral edge, as such defects can cause the edge to flake and become jagged. Particles from flaking edges can break off during subsequent fabrication steps and cause deleterious consequences such as abrading or gouging the surface during polishing steps, adhering to and masking portions of the semiconductor surface during etching steps, contaminating cleaning baths and other wafers therein, and creating reference inaccuracies in lithographic patterning and handling steps.

The peripheral edge of the semiconductor layer is typically removed, before the semiconductor layer is finished in terms of thickness, thickness variation and surface roughness, by abrading, grinding, and/or etching and is usually left at an angle or contour which minimizes the trapping of particles during subsequent exposure to a polishing slurry. For example, Japanese Patent Application No. 07-045485 discloses edge trimming a bonded wafer by abrading with a diamond grinding tool and/or by etching. U.S. Patent No. 5,340,435 to Ito et al. discloses rough grinding the surface of the semiconductor layer and etching the periphery of the ground surface.

Such edge trimming processes which employ only grinding methods, however, typically do not fully preserve the integrity of the insulating layer immediately adjacent the peripheral edge of the trimmed semiconductor layer. The insulating layer which underlies the peripheral edge of the semiconductor layer is generally at least partially removed therewith to ensure complete removal of the semiconductor layer about its edge. As a result, at least part of the peripheral edge of the insulating layer is flush with the peripheral edge of the trimmed semiconductor layer. This becomes problematic during device fabrication steps where the wafers are subjected to conditions which would etch the exposed peripheral edge of the insulating layer, and thereby undercut the semiconductor layer.

Prior art edge-trimming processes which employ grinding and etching also suffer from certain disadvantages. Typically, the grinding step leaves a coarse, rough surface on the semiconductor. When this surface is etched, the etchant may nonuniformly break through the semiconductor layer, thereby exposing the underlying oxide layer to the etchant for varying periods of time and causing irregularities in the exposed surface

of the underlying oxide. Hence, the risk of localized break-through to the underlying substrate layer is heightened. Moreover, where the edge-trimming process exposes a portion of the underlying substrate layer, either by grinding or by break-through etching, subsequent fabrication steps may stain the exposed portion and produce a wafer which is at least cosmetically less desirable.

Where the semiconductor layer is finished after the edge is trimmed, the semiconductor surface has a periphery which is excessively rounded, tapered or beveled, as shown in Figures 11(a) through 11(c). Such a tapered-edge leads to reference inaccuracies in lithographic patterning and handling steps. Additionally, the area of the semiconductor surface suitable for device fabrication is decreased. Moreover, the edge profile must typically be angled or contoured to reduce the accumulation of particulate buildup during polishing.

Further, edge trimming processes known in the art are not suited to a semiconductor-on-insulator wafer having a polished semiconductor surface. Abrasive edge trimming methods employ organic masks such as teflon, polyethylene, waxes or high-molecular weight organic films to protect the exposed semiconductor surface while the edge is abraded, and etching methods employ such masks to block the area of the semiconductor surface not being etched. These conventional masks may contaminate the surface of the semiconductor layer with organic residues.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an edge trimming process in which the areas trimmed and areas excluded from being trimmed are readily controllable, the substrate wafer is not trimmed, abraded

or altered, and the integrity of the insulating layer immediately adjacent the peripheral edge of the semiconductor layer is preserved. It is also an object of the invention to provide a process which is less sensitive to variations in the thickness of the insulating or semiconductor layers between different wafers and which is suitable for batch processing and for use on semiconductor-on-insulator wafers having a polished or etched semiconductor surface. A further object of the invention is to provide a semiconductor-on-insulator wafer having an underlying insulating layer adjacent to the peripheral edge of the semiconductor layer, having a polished surface free of contaminants, having a surface which is not tapered, beveled or rounded at its peripheral edge and being free from polishing slurry without additional process steps to contour the edge profile.

Briefly, therefore, the present invention is directed to a process for trimming the peripheral edge of a semiconductor-on-insulator wafer having, in succession, a substrate layer, an insulating layer and a semiconductor layer which has a first surface adjacent the insulating layer and a second surface parallel to and opposing the first surface. The process comprises forming a masking layer on the second surface of the semiconductor layer wherein the second surface has a RMS surface roughness of less than about 1 μm over an area of about or less than 625 μm^2. The masking layer covers all of the second surface except for an edge margin thereof. The uncovered peripheral portion of the semiconductor layer is etched without substantially etching the masking layer.

In another embodiment, the process comprises forming a masking layer on the second surface of the semiconductor layer, the masking layer covering all of the second surface except for an edge margin thereof and

etching the semiconductor layer to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer. After etching, the masking layer is removed from the second surface of the semiconductor layer and the thickness of the semiconductor layer is reduced by about or less than about 1 μm.

In an additional embodiment of the process, a masking layer is formed over the entire second surface of the semiconductor layer and a protective film is deposited over the masking layer. A peripheral portion of the film is removed to expose a peripheral portion of the underlying masking layer, which, in turn, overlies the edge margin of the semiconductor layer. The exposed peripheral portion of the masking layer is then etched with an etchant that preferentially etches the masking layer over the semiconductor layer to remove the peripheral portion of the masking layer and thereby expose the edge margin of the semiconductor layer. The uncovered portion of the semiconductor layer is then etched without substantially etching the masking layer and without substantially etching the insulating layer.

In a further embodiment of the process, the semiconductor layer has a thickness of less than about 50 μm and the second surface of the semiconductor layer has a RMS surface roughness of less than about 1 μm per an area of about 625 μm^2. A masking layer is formed over the entire second surface of the semiconductor layer and a protective film is deposited over the masking layer. A peripheral portion of the protective film is then removed to expose a peripheral portion of the underlying masking layer, the exposed peripheral portion including the area of the masking layer which overlies the edge margin of the semiconductor layer. The exposed peripheral portion of the masking layer is etched with an etchant which preferentially etches the masking layer over the

semiconductor layer to remove the peripheral portion of the masking layer and to thereby expose the edge margin of the semiconductor layer. The semiconductor layer is then etched to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer. After etching the semiconductor layer, the masking layer is removed from the second surface of the semiconductor layer and thereafter, the thickness of the semiconductor layer is reduced by less than about 1 μm.

The invention is further directed to a semiconductor-on-insulator wafer comprising a substrate layer having a first surface and a second surface parallel to and opposing the first surface, an insulating layer having a first surface adjacent the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface and a mean thickness. The second surface of the semiconductor layer has a radius, r_2, overlying a corresponding radius on the first surface of the semiconductor layer, r_1, and the difference in radii, $r_1 - r_2$, is less than about ten times the mean thickness of the semiconductor layer.

The invention is also directed to a bonded semiconductor-on-insulator wafer comprising a substrate layer having a first surface and a second surface parallel to and opposing the first surface, an insulating layer having a first surface adjacent to the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface and a mean thickness. The first surface of the semiconductor layer

has a radius, r_1 and a characterizing radius, r_c, which is equal to r_1 less a distance of about ten times the mean thickness of the semiconductor layer. The thickness of the semiconductor layer measured at its characterizing radius, r_c, is about equal to the mean thickness of the semiconductor layer.

The invention is directed, moreover, to a semiconductor on insulator wafer comprising a substrate layer having a first surface and a second surface parallel to and opposing the first surface, an insulating layer having a first surface adjacent the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface and a mean thickness ranging from about 100 Å to about 50 μm with a maximum total thickness variation of less than about 15% of the mean thickness of the semiconductor layer. The second surface of the semiconductor layer has a radius, r_2, overlying a corresponding radius on the first surface of the semiconductor layer, r_1, which also has a characterizing radius, r_c, defined as r_1 less a distance of about ten times the mean thickness of the semiconductor layer. The difference in radii, $r_1 - r_2$, is less than about ten times the mean thickness of the semiconductor layer, and the thickness of the semiconductor layer measured at its characterizing radius, r_c, is about equal to the mean thickness of the semiconductor layer. The entire first surface of the semiconductor layer is generally uniformly bonded to the second surface of the insulating layer, and the bond formed between the semiconductor layer and the insulating layer is characterized by a lack of peripheral lamination defects.

Other objects and features of the present invention will be in part apparent to those skilled in the art and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a) and 1(b) are perspective and schematic cross-sectional views, respectively, of an untrimmed semiconductor-on-insulator wafer.

Fig. 2 is a schematic cross-sectional view of an untrimmed semiconductor-on-insulator wafer having intermediate layers.

Figs. 3(a) through 3(e) are views of a semiconductor-on-insulator wafer at various stages of the edge-trimming process of the present invention. Figs. 3(a), 3(c) and 3(d) are schematic cross-sectional views. Fig. 3(b) is a top plan view. Fig. 3(e) is a perspective view of a trimmed semiconductor-on-insulator wafer.

Figs. 4(a) through 4(d) are schematic cross-sectional views of a semiconductor-on-insulator wafer at various stages of a method for forming a masking layer over all but the edge margin of the surface of the semiconductor layer.

Figs. 5(a) and 5(b) are schematic cross-sectional views of a semiconductor-on-insulator wafer at various stages of another method for forming a masking layer over all but the edge margin of the surface of the semiconductor layer.

Figs. 6(a) through 6(d) are schematic cross-sectional views of semiconductor-on-insulator wafers differing in the extent to which the insulating layer covers the substrate layer.

Fig. 7 is a schematic cross-sectional view of a trimmed semiconductor-on-insulator wafer showing the area enlarged in Fig. 8.

Figs. 8(a) through 8(c) are enlarged schematic cross-sectional views of the peripheral edge of the trimmed semiconductor layer shown in Fig. 7.

Figs. 9(a) and 9(b) are cut-away schematic cross-sectional views of the right half of the trimmed semiconductor-on-insulator wafer shown in Fig. 7.

Fig. 10 is a graph showing the edge profile of a trimmed semiconductor-on-insulator wafer.

Figs. 11(a) through 11(c) are enlarged schematic cross-sectional views of the peripheral edge of a semiconductor-on-insulator wafer edge-trimmed according to prior art methods.

DETAILED DESCRIPTION OF THE INVENTION

In the present invention, the peripheral edge of a semiconductor-on-insulator wafer is trimmed by forming a differentially etchable masking layer over all but the edge margin of the surface of the semiconductor layer and selectively etching the peripheral portion of the semiconductor layer without removing the insulating layer. The process may be applied to a bonded semiconductor-on-insulator wafer to remove lamination defects located between the semiconductor layer and the insulating layer.

Advantageously, the semiconductor-on-insulator wafer is close to being in its finished state before being edge-trimmed. That is, the thickness, thickness variation, surface roughness and surface defects of the semiconductor layer approximate, before edge-trimming, the same characteristics of a wafer in its final, finished form which is suitable for device fabrication. Specifically, before edge-trimming according to the present invention, the thickness of the semiconductor layer has been reduced to less than about 50 μm and the total thickness variation of the untrimmed semiconductor layer is less than about 1 μm. The surface of the

untrimmed semiconductor layer has been etched or polished and has a surface roughness which is less than that of a typical ground surface. Preferably, the semiconductor layer has a root-mean-square (RMS) surface roughness of less than about 1 μm per an area of about 625 μm^2 and most preferably less than about 1 μm over an area of about 400 μm^2.

Because of the relative smoothness of the surface being etched as compared to ground surfaces, the etching of the periphery proceeds uniformly such that the underlying insulating layer, which acts as an etch stop, is not subject to local variation in the extent to which it is exposed to the etchant. A similar advantage results from having a small thickness variation. Together, the result is a more uniform insulating layer outside the periphery of the edge-trimmed semiconductor layer and a marked decrease in the likelihood of breakthrough during etching.

A further advantage arising out of the aforementioned characteristics of the semiconductor layer is that only minimal additional polishing is required after edge-trimming to create a finished wafer which is ready for device fabrication. As a result, the edge-trimmed semiconductor-on-insulator wafer is characterized by its semiconductor layer being free from tapering, beveling and/or rounding near its periphery. The resulting sharp-edged semiconductor layer improves the accuracy of lithographic patterning and handling by providing a more representative reference edge, and also maximizes the surface area available for device fabrication. Bonded semiconductor-on-insulator wafers are further characterized by a lack of peripheral lamination defects.

The invention is described in further detail below with reference to the figures, in which like items are numbered the same in the several figures.

Referring to Figs. 1(a) and 1(b), an untrimmed semiconductor-on-insulator wafer 2 comprises, in succession, a substrate layer 10, an insulating layer 20 and a semiconductor layer 30. In an alternative embodiment shown in Fig. 2, the semiconductor-on-insulator wafer 2 may also comprise one or more intermediate layers 40, 42, situated between the insulating layer 20 and the semiconductor layer 30.

The substrate layer 10 has first and second parallel and opposing surfaces 11, 12 and a generally circular peripheral side 14. The peripheral side may include an orientation flat, notch or other means for identifying wafer orientation. The substrate layer 10 may be any material suitable for support and handling, including, for example, a semiconductor material such as silicon, a compound semiconductor material, polycrystalline silicon, glass materials such as fused quartz and ceramic materials such as alumina, aluminum oxide or silicon nitride. The conductivity type and resistivity are not critical. The substrate layer 10 may be patterned or unpatterned and may be of any desired thickness. Although thickness control is not critical for practicing the present invention, a uniform thickness is generally desirable for handling during device fabrication steps. The total thickness variation of the substrate layer is preferably less than about 10 μm.

The insulating layer 20 has a first surface 21 adjacent the second surface 12 of the substrate layer 10 and a second surface 22 parallel to and opposing the first surface 21. The insulating layer also has a peripheral side 24. The insulating layer 20 is preferably silicon dioxide, silicon nitride or combinations thereof, and most preferably a thermally grown silicon dioxide. The thickness of the insulating layer 20 is not critical but it preferably ranges from about 5 Å (0.5 nm) to about 5 mm. Thickness control of

the insulating layer is likewise not critical for practicing the present invention, but total thickness variation is preferably less than about 10 μm.

The semiconductor layer 30 has a first surface 31 adjacent the second surface 22 of the insulating layer 20, a second surface 32 parallel to and opposing the first surface 31, and a peripheral side 34. The second surface 32 has an edge margin 36. The semiconductor layer 30 may be any type of semiconductor material, compound semiconductor material or doped semiconductor material. Silicon is a preferred semiconductor material. The semiconductor layer has a mean thickness which is equal to the mean perpendicular linear distance between the second surface 32 and the first surface 31 of the semiconductor layer. The thickness of the semiconductor layer 30 preferably ranges from about 100 angstroms (10 nm) to about 50 μm and is preferably within about 1 μm of its final thickness before edge-trimming according to the present invention, such that after edge-trimming, the semiconductor layer 30 preferably requires a reduction in its thickness of less than about 1 μm. The reduction in thickness after edge-trimming is more preferably less than about 0.5 μm (5000 Å) and most preferably less than about 0.3 μm (3000 Å). The total thickness variation of the semiconductor layer 30 is preferably less than about 5 μm, more preferably less than about 2 μm and most preferably less than about 1 μm. In terms of mean thickness, the total thickness variation is preferably less than about 15% of the mean thickness.

The second surface 32 may have an etched or polished finish prior to the edge trimming process of the present invention and is preferably polished to a specular gloss finish. The second surface 32 should be free from crystallographic defects such as surface dislocations which typically result from conventional grinding processes. The microroughness of the second surface 32

should have a smaller short-range variation and be less rough than conventionally ground surfaces. Specifically, the second surface 32 should have, prior to being edge-trimmed, a RMS surface roughness of less than about 1 μm over an area of about 625 μm^2. The surface roughness of the second surface 32 is more preferably less than about 0.5 μm, even more preferably less than about 1 nm and most preferably less than about 1 Å (0.1 nm) over such an area.

When the semiconductor-on-insulator wafer 2 includes intermediate layers 40, 42, the first surface 31 of the semiconductor layer 30 is adjacent the intermediate layer 42. The intermediate layers 40, 42 may be metallic materials, refractory metal silicides, other semiconductor materials, compound semiconductor materials, polycrystalline silicon, doped silicon or ceramic materials such as sapphire or silicon carbide.

In one embodiment, the semiconductor-on-insulator wafer 2 is a bonded semiconductor-on-insulator wafer in which a silicon dioxide insulating layer 20 is formed over the second surface 12 of the substrate layer 10, by thermal growth for example, and in which the first surface 31 of the semiconductor layer 30 is bonded to the second surface 22 of the insulating layer. Lamination defects located around the periphery of the bond formed between the insulating layer 20 and the semiconductor layer 30 may occur due to irregularities in the shape of the unbonded layers near their periphery, defects caused by handling the unbonded layers or impurities being swept to the edge during the bonding process.

Referring to Figure 3(a), a masking layer 50 is formed on the second surface 32 of the semiconductor layer 30. The masking layer 50 is preferably a material which is capable of being etched at an etch rate which differs from the etch rate of the semiconductor layer 30, preferably by a factor of at least 100. For example,

when it is desired to remove the semiconductor layer 30 preferentially to the masking layer 50, the etch rate of the semiconductor layer 30 is preferably at least 100 times greater than the etch rate of the masking layer. Conversely, if it is desired to leave the semiconductor layer 30 while preferentially removing the masking layer 50, the etch rate of the semiconductor layer 30 is preferably at least about 100 times less than the etch rate of the masking layer. Suitable materials for the masking layer 50 include silicon dioxide, silicon nitride, silicides, molybdenum, aluminum, or etch-resistant organic masking materials. Materials which would leave a residue on the second surface 32 of the semiconductor layer 30 and which would require polishing or further process steps to remove are less preferred. Silicon dioxide is a preferred material for the masking layer 50.

Silicon dioxide and silicon nitride masking layers 50 are formed on the second surface 32 of the semiconductor layer 30 by techniques known in the art, including thermal growth, evaporation, chemical vapor deposition and plasma enhanced deposition. Silicon dioxide is preferably formed on the masking layer 50 by thermal growth processes. Silicides are formed on the semiconductor layer 30 by chemical vapor deposition or by thermal treatment of deposited metals. Metals such as molybdenum and aluminum are formed on the semiconductor layer 30 by vapor deposition or evaporation methods. The thickness of the masking layer 50 formed on the semiconductor layer 30 ranges from about 10 angstroms (1 nm) to about 1000 angstroms (100 nm), depending on the thickness of the semiconductor layer and on the difference in the etch rate of the masking layer versus that of the semiconductor layer. A 50 Å (5 nm) thick SiO_2 masking layer is appropriate for use over a 2000 Å (0.2 μm) thick silicon layer, whereas relatively thicker

layers, such as a 400 Å (40 nm) thick SiO_2 masking layer, may be appropriate over a 4.5 μm thick silicon layer. The masking layer 50 is preferably free from pinhole defects which would reduce its effectiveness as a mask. The masking layer is also preferably free of other defects such as edge variation, edge crown, delamination or particulates which would limit its use in defining a smooth edge.

The masking layer 50 covers all of the second surface 32 of the semiconductor layer 30 except for the edge margin 36 thereof. As shown in Fig. 3(b), the width, w, of the uncovered edge margin 36 defines the peripheral portion of the semiconductor layer 30 to be removed and ranges from about 0.5 mm to about 10 mm. For bonded wafers, the width of the edge margin should be sufficient to ensure that peripheral lamination defects are removed during subsequent steps. The edge margin width, w, is preferably less than about 3 mm and most preferably less than about 1mm.

Referring to Figures 4(a) through 4(d), one method for covering all but the edge margin 36 of the second surface 32 of the semiconductor layer 30 with the masking layer 50 includes first forming a masking layer 50 over the entire second surface 32 of the semiconductor layer 30. (Fig. 4(a)). A protective film 60 is then deposited on the masking layer 50. (Fig. 4(b)). A peripheral portion 62 of the protective film 60 is removed to expose a peripheral portion 52 of the underlying masking layer 50. (Fig. 4(c)). The exposed peripheral portion 52 of the masking layer 50 is then removed by etching with an etchant that preferentially etches the masking layer over the semiconductor layer. (Fig. 4(d)). The protective film 60 may, if desired, be removed. (Fig. 3(a)).

The protective film 60 is an organic or inorganic film patternable by lithographic or mechanical means. Resins and polymers are suitable. Photo-resist or non

photo-resist films may be employed, depending on the manner in which the peripheral portion 62 of the protective film 60 is to be removed during subsequent steps. The protective film 60 is deposited by spinning it on to the masking layer 50, preferably to a thickness ranging from about 1 μm to about 3 μm.

The peripheral portion 62 of the protective film 60 being removed is that portion which overlies the edge margin 36 of the second surface 32 of the semiconductor layer 30. The peripheral portion 62 is removed by lithographic or mechanical methods known in the art. Lithographic methods may be used to accurately and reproducibly remove photo-resist films, but are relatively expensive. Mechanical methods, such as polishing, are less expensive and may be carried out using edge grinders or edge polishing tools known in the art. If the peripheral portion 62 is removed by mechanical means, the underlying masking layer 50 is preferably a hard material relative to the protective film 60, such as silicon dioxide.

The exposed underlying peripheral portion 52 of the masking layer 50 is removed by etching. The etchant should preferentially etch the masking layer 50 over the semiconductor layer 30 with an etch rate ratio of about 100:1. The ratio of etch rates of the masking layer 50 to semiconductor layer 30 is more preferably greater than about 1,000:1. In a preferred embodiment, in which the underlying semiconductor layer 30 is silicon, a silicon dioxide masking layer 50 may be etched using hydrofluoric acid (HF), preferably with a buffering agent such as ammonium fluoride. Although the concentration of etchant is not critical, an aqueous solution having a molar concentration of HF ranging from about 5% to about 10% will satisfactorily etch the silicon dioxide masking layer 50 at ambient temperatures within a few minutes, without substantially etching the underlying silicon

semiconductor layer 30. A silicon nitride masking layer 50 may be etched using phosphoric acid (H_3PO_4). Although not critical, an aqueous solution having an 85% molar concentration of H_3PO_4 will satisfactorily etch the silicon nitride masking layer 50 at about 150 °C within about 5 minutes, without substantially etching the silicon semiconductor layer 30. Dry etching techniques known in the art could also be used to etch both silicon dioxide and silicon nitride preferentially over silicon.

After etching the exposed peripheral portion 52 of the masking layer 50, the remainder of the protective film 60 may be removed. Methods known in the art, including stripping by oxidizing with sulfuric acid, dissolving in solvent, ashing or grinding can be used to completely remove the protective film 60 from the masking layer 50.

An alternative method for covering all but the edge margin 36 of the second surface 32 of the semiconductor layer 30 with the masking layer 50 includes, as shown in Figures 5(a) and 5(b), covering the edge margin 36 with an annular blocking ring 70, (Fig. 5(a)), forming a masking layer 50 on the uncovered area of the second surface 32 (Fig. 5(b)) and removing the blocking ring 70. (Fig. 3(a)). The annular blocking ring 70 may be of any material which is compatible with the subsequent formation of the masking layer 50 on the uncovered areas of the semiconductor layer 30, including, for example, glass, ceramic, quartz, semiconductors such as silicon and metals. The blocking ring 70 is set onto the surface 32 to cover the edge margin 36. The blocking ring 70 is preferably held in place by gravity, but may also be clamped in place. The masking layer 50 may be formed on the uncovered area of the semiconductor layer surface 32 by any of the methods previously discussed, except that thermal growth is a less preferred technique. The

blocking ring 70 is removed by lifting it off of the surface 32. Other methods employing a similar approach are also envisioned.

Regardless of the method by which the masking layer 50 covers all of the second surface 32 except for the edge margin 36, the semiconductor layer 30 is then etched to remove the uncovered portion of the semiconductor layer 30 without substantially etching the masking layer 50, as shown in Figure 3(c). The etchant should preferentially etch the semiconductor layer 30 over the masking layer 50 with an etch rate ratio greater than about 100:1. The ratio of etch rates of the semiconductor layer 30 to the masking layer 50 is more preferably greater than about 1,000:1. The etchant should etch selectively, but without orientation dependency.

In a preferred embodiment, in which a silicon dioxide masking layer 50 covers a silicon semiconductor layer 30, a suitable etchant is a solution comprising ethylenediamine, pyrocathecol and water. The silicon semiconductor layer 30 is etched in such a ethylenediamine-pyrocathecol-water solution at standard molar concentrations and at a temperature of about 150 °C for a period ranging from about 1/2 minute to a few minutes. Other suitable etchants include potassium hydroxide (KOH) or ammonium hydroxide (NH_4OH) solutions having a molar concentration of hydroxyl ion of about 0.4 M at a temperature of about 180 °C for a period of about 5 minutes. Other etchants, such as hydrazine, ethanolamine-pyrazinamide-gallic acid-water solution, are also known in the art for preferentially etching silicon over silicon dioxide. Dry etching methods known in the art may be employed as well. These same etchants are suitable when silicon nitride is used as the masking layer 50.

The semiconductor layer 30 is preferably etched without substantially etching the insulating layer 20. The etchants discussed above with respect to preferentially etching the semiconductor layer 30 over silicon dioxide or silicon nitride masking layers 50 are equally suitable for etching the semiconductor layer 30 over silicon dioxide or silicon nitride insulating layers 20. If the insulating layer 20 is not the same material as the masking layer 50, then the etchant would have to preferentially etch the semiconductor layer 30 over both the masking layer 50 and the insulating layer 20.

After etching the trimmed semiconductor layer 30 has a new peripheral side 37 contained within the peripheral side 14 of the substrate layer 10, and the second surface 32 of the trimmed semiconductor layer 30 remains covered by the masking layer 50, as shown in Fig. 3(c). The masking layer 50 may be removed, if desired, by mechanical methods or by etching to expose the second surface 32 of the semiconductor layer 30. (Fig. 3(d)). Preferably, the masking layer 50 is removed by preferentially etching the masking layer 50 over the semiconductor layer 30. When the second surface 32 of the semiconductor layer 30 has a specular gloss finish, the etchant should not roughen the surface 32 of the semiconductor layer. Appropriate etchants, such as HF, and etching conditions are discussed above. If the masking layer 50 is the same material as the insulating layer 20 (e.g. silicon dioxide), exposed portions of the insulating layer 20 should be masked to prevent being etched when the masking layer 50 is etched. If desired, however, exposed portions of the insulating layer could be removed by etching at the same time that the masking layer is etched.

If the semiconductor-on-insulator wafer 2 comprises intermediate layers 40, 42, the semiconductor layer 30 may be etched without substantially removing these

intermediate layers. Alternatively, the intermediate layers 40, 42 may also be etched to remove a peripheral portion thereof underlying the portion of the semiconductor layer removed.

The substrate layer 10 is preferably unaffected by any of the process steps discussed above. The substrate layer 10 is not abraded, etched or otherwise altered in thickness or in edge profile. Appropriate steps known to those skilled in the art, such as masking any portions of the substrate layer 10 potentially exposed to more than substantial etching, should be employed. The thickness and edge profile of the substrate layer 10 should be maintained to ensure compatibility with handling equipment and lithographic tooling and to preclude damage propagation and particle shedding during subsequent processing steps.

After edge-trimming and removal of the masking layer 50, the second surface 32 of the semiconductor layer may be touch-polished or otherwise finished to achieve a desired surface finish. Regardless of the finishing means, the thickness of the edge-trimmed semiconductor layer is preferably reduced by less than about 1 μm.

Semiconductor-on-insulator wafers manufactured by the method described above have several important characteristics. As shown in Figs. 3(d) and 3(e), the insulating layer 20 includes a peripheral portion 26 lying outside the peripheral side 37 of the semiconductor layer 30. The peripheral portion 26 of the insulating layer 20 protects the semiconductor layer 30 from being undercut during subsequent device fabrication steps in which the insulating layer 20 could be etched out from under the semiconductor layer 30. As shown in Fig. 6(a), the insulating layer 20 need not extend to the peripheral side 14 of the substrate layer 10. Figs. 6(b)-6(d) show further variations in which the semiconductor-on-insulator wafer 2 could also include an insulating layer

20 covering the entire first surface 11 of the substrate layer 10 (Fig. 6(b)), covering the peripheral side 14 of the substrate layer 10 (Fig. 6(c)) or covering the entirety of the substrate layer 10 (Fig. 6(d)). The insulating layer 20 overlying these surfaces is preferably formed before the semiconductor-on-insulator wafer 2 is trimmed according the process of the present invention.

Moreover, when the second surface 32 of the semiconductor layer 30 is, as described above, polished or etched prior to edge trimming, the tapering, beveling and/or rounding effects associated with prior art edge-trimming methods are eliminated. Referring to Figs. 7 through 10, the semiconductor-on-insulator wafers trimmed according to the present invention have a sharp-edged semiconductor layer 30. The first and second surfaces 31, 32 of the semiconductor layer 30 have first and second peripheral edges, 38, 39 respectively, which are coplanar with their respective surfaces 31, 32. As shown in Figures 8(a) through 8(c), the edge profile or contour of the peripheral side 37 is not critical. The edge profile may be generally convex, straight or concave and may be irregular or smooth.

The sharp-edged semiconductor layer 30 is characterized by the difference in the length of radii on the first and second surfaces 31, 32. As shown in Figure 9(a), the distance from the center of the second surface 32 to the second peripheral edge 39 defines a radius, r_2, which overlies a corresponding radius, r_1, on the first surface 31 of the semiconductor layer 30, defined by the distance from the center of the first surface 31 to the first peripheral edge 38. The difference in radii, $r_1 - r_2$, referred to in the figures as Δr, is preferably less than about ten times the mean thickness of the

semiconductor layer 30, more preferably less than about two times the mean thickness of the semiconductor layer 30, and most preferably about equal to or less than the mean thickness of the semiconductor layer 30.

This sharp-edged feature may also be characterized in terms of the thickness of the semiconductor layer at a characterizing radius, r_c, relative to the mean thickness of the semiconductor layer. As shown in Figure 9(b), the characterizing radius, r_c is defined as the radius r_1 of the first surface 31 less a distance x, $r_1 - x$, where x is preferably about ten times the mean thickness of the semiconductor layer 30, more preferably about two times the mean thickness of the semiconductor layer 30, and most preferably about equal to or less than the mean thickness of the semiconductor layer 30. The thickness of the semiconductor layer 30 measured at its characterizing radius, r_c, is about equal to the mean thickness of the semiconductor layer 30. Although the sharp-edged semiconductor-on-insulator wafer of the present invention has been characterized in terms of radii, analogous characterizations are applicable for non-circular wafers.

In the bonded semiconductor-on-insulator wafer embodiment in which the silicon dioxide insulating layer 20 is formed over the second surface 12 of the substrate layer 10 and the first surface 31 of the semiconductor layer 30 is bonded to the second surface 22 of the insulating layer, the bond integrity is consistent throughout the bonded area. The entire first surface 31 is generally uniformly bonded to the second surface 22 and the bond formed therebetween is characterized by a lack of peripheral lamination defects.

In light of the detailed description of the invention, it can be appreciated that the several objects of the invention are achieved. The explanations and illustrations presented herein are intended to acquaint

others skilled in the art with the invention, its principles, and its practical application. Those skilled in the art may adapt and apply the invention in its numerous forms, as may be best suited to the requirements of a particular use. Accordingly, the specific embodiments of the present invention as set forth are not intended as being exhaustive or limiting of the invention.

CLAIMS

WHAT IS CLAIMED IS:

1. A process for trimming the peripheral edge of a semiconductor-on-insulator wafer having, in succession, a substrate layer, an insulating layer and a semiconductor layer, the semiconductor layer having a first surface adjacent the insulating layer and a second surface parallel to and opposing the first surface, the process comprising

forming a masking layer on the second surface of the semiconductor layer, the second surface of the semiconductor layer having a RMS surface roughness of less than about 1 μm per an area of about 625 μm^2, the masking layer covering all of the second surface except for an edge margin thereof, and

etching the semiconductor layer to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer.

2. The process as set forth in claim 1 further comprising

after etching, removing the masking layer from the second surface of the semiconductor layer and

after removing the masking layer, reducing the thickness of the semiconductor layer by less than about 1 μm.

3. The process as set forth in claim 1 wherein the thickness of the semiconductor layer, prior to forming a masking layer thereover, is less than about 50 μm.

4. The process as set forth in claim 1 wherein, prior to forming the masking layer thereover, the second surface of the semiconductor layer has a specular gloss finish.

5. The process as set forth in claim 1 wherein the masking layer is preferentially etchable over the semiconductor layer by a factor of at least about 100.

6. The process as set forth in claim 1 wherein the masking layer comprises silicon dioxide or silicon nitride.

7. The process as set forth in claim 1 wherein the step of forming a masking layer on the second surface of the semiconductor layer comprises

forming a masking layer over the entire second surface of the semiconductor layer,

depositing a protective film on the masking layer,

removing a peripheral portion of the protective film to expose a peripheral portion of the underlying masking layer, the exposed peripheral portion including the area of the masking layer which overlies an edge margin of the semiconductor layer, and

etching the exposed peripheral portion of the masking layer with an etchant which preferentially etches the masking layer over the semiconductor layer to remove the peripheral portion of the masking layer and thereby expose the edge margin of the semiconductor layer.

8. The process as set forth in claim 1 wherein the semiconductor-on-insulator wafer has at least one intermediate layer between the insulating layer and the semiconductor layer, the first surface of the semiconductor layer being adjacent the intermediate layer.

9. A process for trimming the peripheral edge of a semiconductor-on-insulator wafer having, in succession, a substrate layer, an insulating layer and a semiconductor layer, the semiconductor layer having a first surface

adjacent the insulating layer and a second surface parallel to and opposing the first surface, the process comprising

forming a masking layer on the second surface of the semiconductor layer, the masking layer covering all of the second surface except for an edge margin thereof, and

etching the semiconductor layer to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer,

after etching, removing the masking layer from the second surface of the semiconductor layer and

after removing the masking layer, reducing the thickness of the semiconductor layer by about or less than about 1 μm.

10. The process as set forth in claim 9 wherein before the masking layer is formed on the semiconductor layer, the semiconductor layer has a thickness of less than about 50 μm.

11. The process as set forth in claim 9 wherein before the masking layer is formed on the semiconductor layer, the maximum total thickness variation of the semiconductor layer is less than about 1 μm.

12. A process for trimming the peripheral edge of a semiconductor-on-insulator wafer having, in succession, a substrate layer, an insulating layer and a semiconductor layer, the semiconductor layer having a first surface adjacent the insulating layer, a second surface parallel to and opposing the first surface and an edge margin, the process comprising

forming a masking layer over the entire second surface of the semiconductor layer,

depositing a protective film over the masking layer,

removing a peripheral portion of the protective film to expose a peripheral portion of the underlying masking layer, the exposed peripheral portion including the area of the masking layer which overlies the edge margin of the semiconductor layer,

etching the exposed peripheral portion of the masking layer with an etchant which preferentially etches the masking layer over the semiconductor layer to remove the peripheral portion of the masking layer and thereby expose the edge margin of the semiconductor layer, and

etching the semiconductor layer to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer.

13. A process for trimming the peripheral edge of a semiconductor-on-insulator wafer having, in succession, a substrate layer, an insulating layer and a semiconductor layer, the semiconductor layer having a first surface adjacent the insulating layer, a second surface parallel to and opposing the first surface and an edge margin, the process comprising

forming a masking layer over the entire second surface of the semiconductor layer, the semiconductor layer having a thickness of less than about 50 μm and the second surface of the semiconductor layer having a RMS surface roughness of less than about 1 μm per an area of about 625 μm^2,

depositing a protective film over the masking layer,

removing a peripheral portion of the protective film to expose a peripheral portion of the underlying masking layer, the exposed peripheral portion including the area of the masking layer which overlies the edge margin of the semiconductor layer,

etching the exposed peripheral portion of the masking layer with an etchant which preferentially etches the masking layer over the semiconductor layer to remove

the peripheral portion of the masking layer and thereby expose the edge margin of the semiconductor layer,

etching the semiconductor layer to remove the uncovered portion of the semiconductor layer without substantially etching the masking layer,

after etching the semiconductor layer, removing the masking layer from the second surface of the semiconductor layer and

after removing the masking layer, reducing the thickness of the semiconductor layer by less than about 1 μm.

14. A semiconductor-on-insulator wafer comprising

a substrate layer having a first surface and a second surface parallel to and opposing the first surface,

an insulating layer having a first surface adjacent the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and

a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface and a mean thickness, the second surface of the semiconductor layer having a radius, r_2, overlying a corresponding radius on the first surface of the semiconductor layer, r_1,

the difference in radii, $r_1 - r_2$, being less than about ten times the mean thickness of the semiconductor layer.

15. The semiconductor-on-insulator wafer of claim 14 wherein the entire first surface of the semiconductor layer is generally uniformly bonded to the second surface of the insulating layer, the bond formed between the semiconductor layer and the insulating layer being characterized by a lack of peripheral lamination defects.

16. The semiconductor-on-insulator wafer of claim 14 wherein the mean thickness of the semiconductor layer ranges from about 10 nm to about 50 μm with a thickness variation of less than about 15% of the mean thickness.

17. The semiconductor-on-insulator wafer of claim 14 wherein the semiconductor layer has a characterizing radius, r_c, the characterizing radius being equal to r_1 less a distance of about ten times the mean thickness of the semiconductor layer, the thickness of the semiconductor layer measured at its characterizing radius, r_c, being about equal to the mean thickness of the semiconductor layer.

18. The semiconductor-on-insulator wafer of claim 14 wherein the semiconductor layer has a peripheral side and the insulating layer includes a peripheral portion lying outside the peripheral side of the semiconductor layer.

19. The semiconductor-on-insulator wafer of claim 14 wherein the insulating layer is an insulating layer formed over the entirety of the substrate layer.

20. The semiconductor-on-insulator wafer of claim 14 further comprising one or more intermediate layers between the second surface of the insulating layer and the semiconductor layer, the first surface of the semiconductor layer being adjacent the intermediate layer.

21. A semiconductor-on-insulator wafer comprising a substrate layer having a first surface and a second surface parallel to and opposing the first surface,

an insulating layer having a first surface adjacent the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and

a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface and a mean thickness, the first surface of the semiconductor layer having a radius, r_1 and a characterizing radius, r_c, the characterizing radius being equal to r_1 less a distance of about ten times the mean thickness of the semiconductor layer,

the thickness of the semiconductor layer measured at its characterizing radius, r_c, being about equal to the mean thickness of the semiconductor layer.

22. A semiconductor-on-insulator wafer comprising

a substrate layer having a first surface and a second surface parallel to and opposing the first surface,

an insulating layer having a first surface adjacent the second surface of the substrate layer and a second surface parallel to and opposing the first surface, and

a semiconductor layer having a first surface adjacent the second surface of the insulating layer, a second surface parallel to and opposing the first surface, and a mean thickness ranging from about 100 Å to about 50 μm with a maximum total thickness variation of less than about 15% of the mean thickness, the second surface of the semiconductor layer having a radius, r_2, overlying a corresponding radius on the first surface of the semiconductor layer, r_1, the first surface also having a characterizing radius, r_c, defined as r_1 less a distance of about ten times the mean thickness of the semiconductor layer,

the difference in radii, $r_1 - r_2$, being less than about ten times the mean thickness of the semiconductor layer,

the thickness of the semiconductor layer measured at its characterizing radius, r_c, being about equal to the mean thickness of the semiconductor layer, and

the entire first surface of the semiconductor layer being generally uniformly bonded to the second surface of the insulating layer, the bond formed between the semiconductor layer and the insulating layer being characterized by a lack of peripheral lamination defects.

FIG. 1(a)

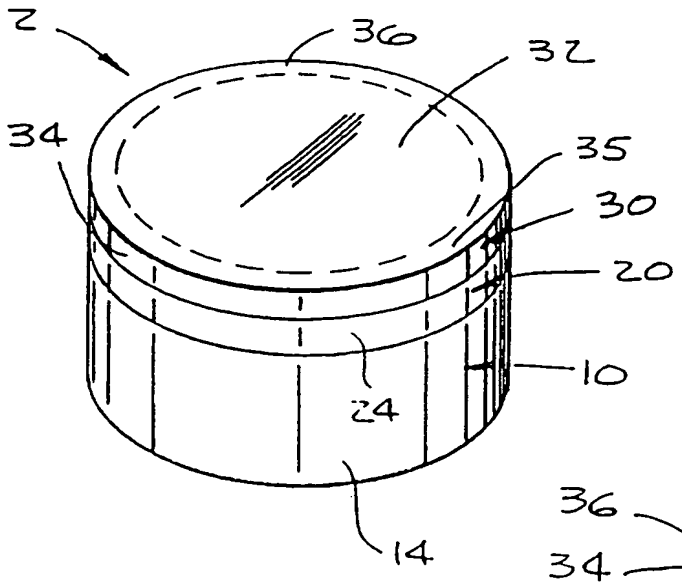


FIG. 1(b)

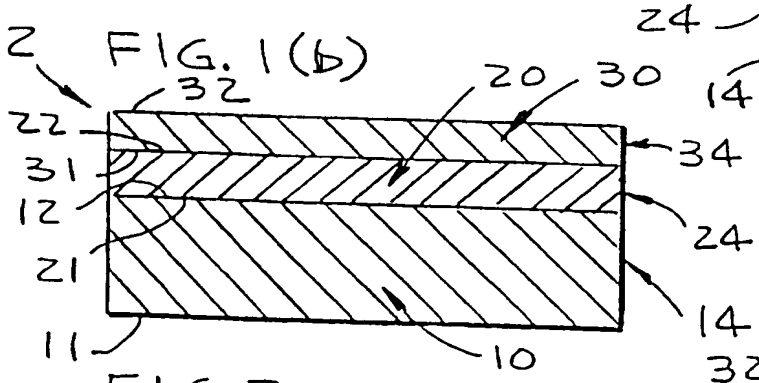


FIG. 2

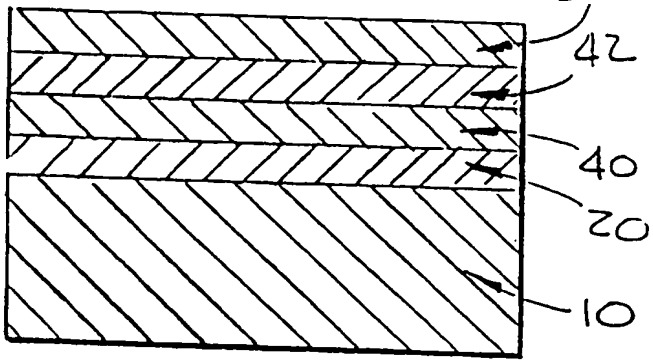


FIG. 3(a)

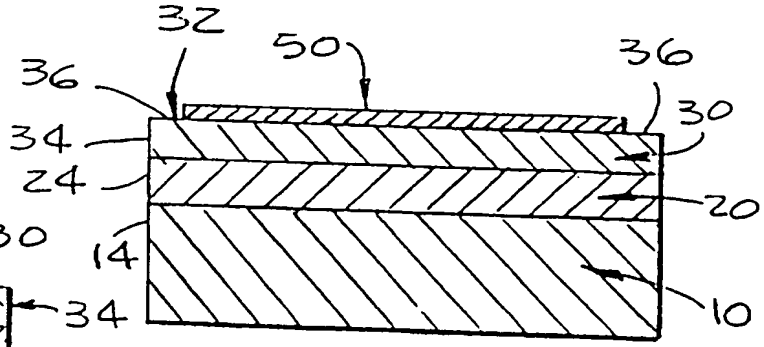


FIG. 3(b)

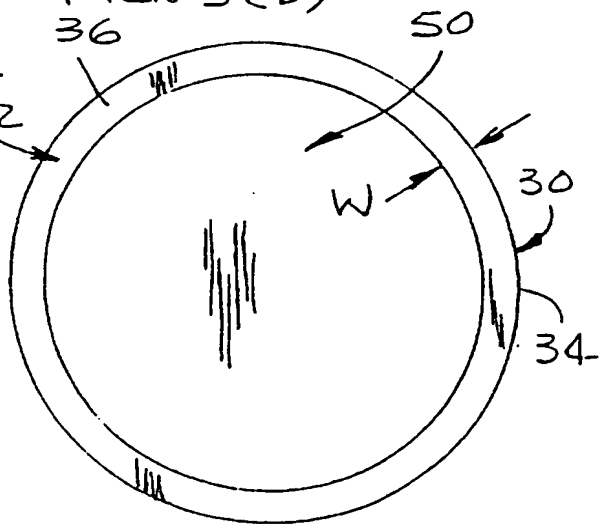


FIG. 3(c)

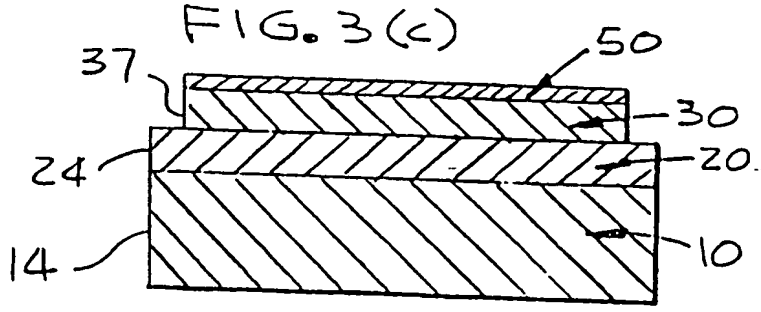


FIG. 3(d)

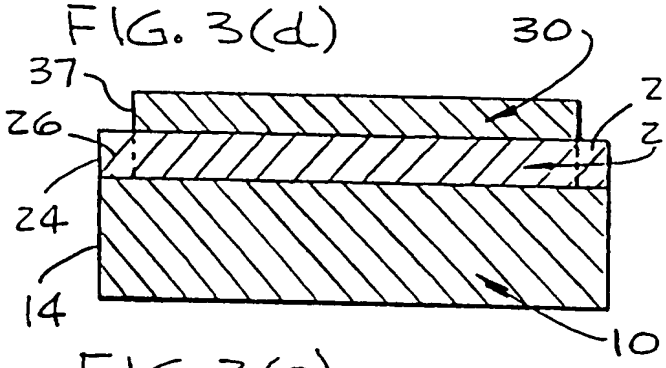


FIG. 3(e)

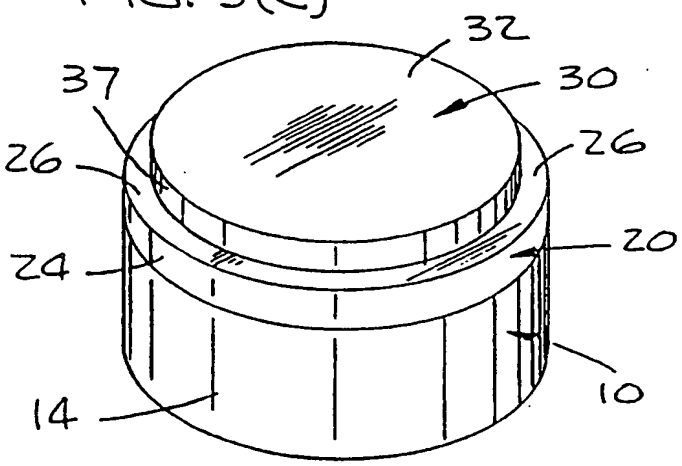
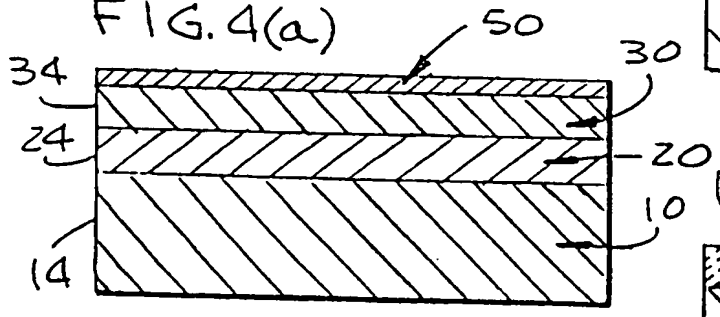


FIG. 4(a)



62 FIG. 4(b)

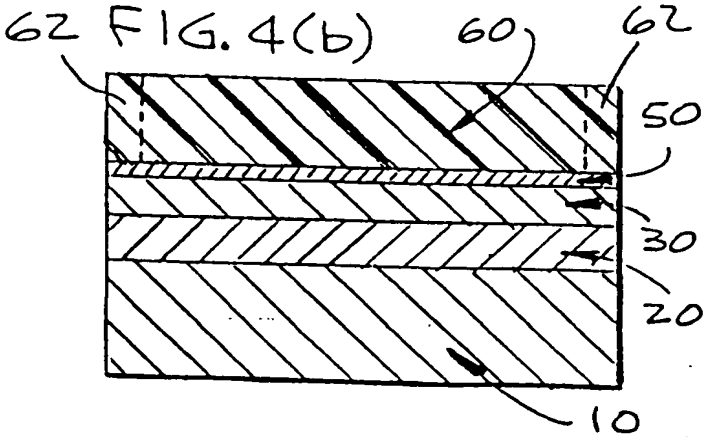


FIG. 4(c)

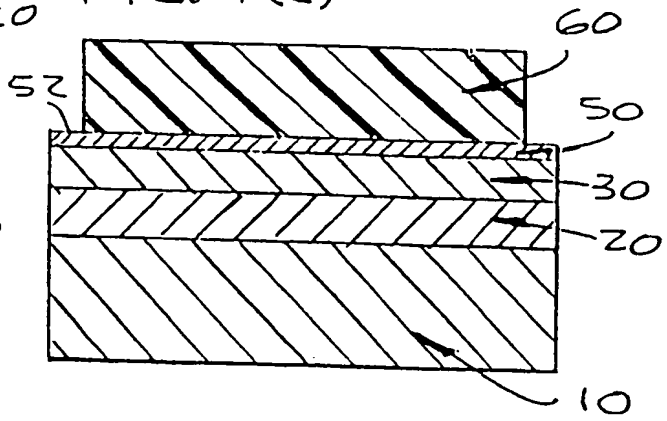


FIG. 4(d)

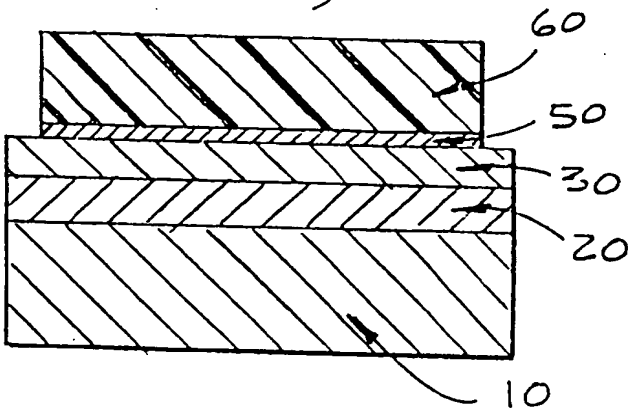


FIG. 5(a)

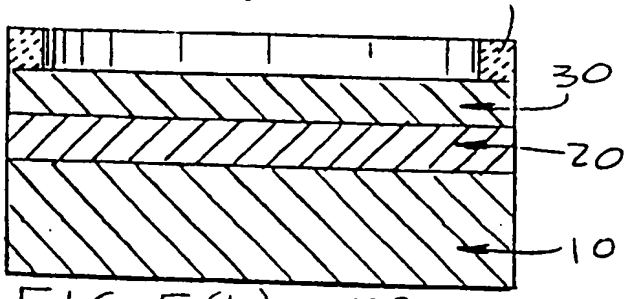


FIG. 5(b)

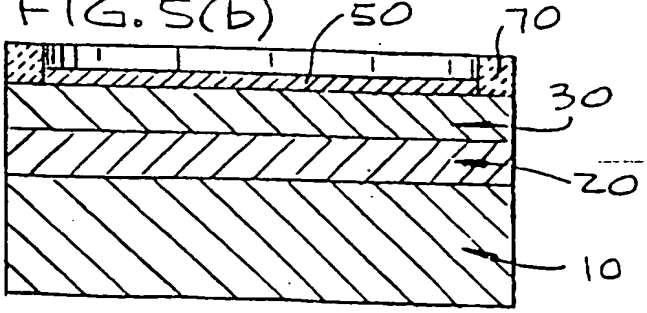


FIG.6(a)

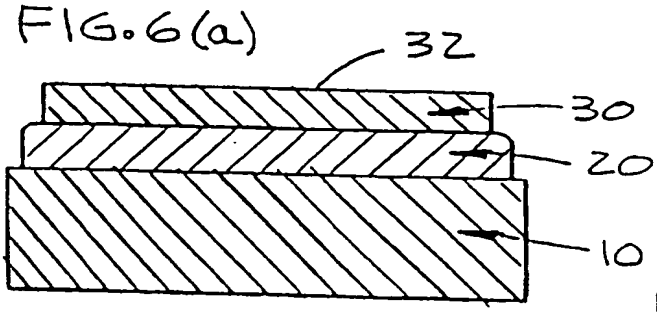


FIG.6(b)

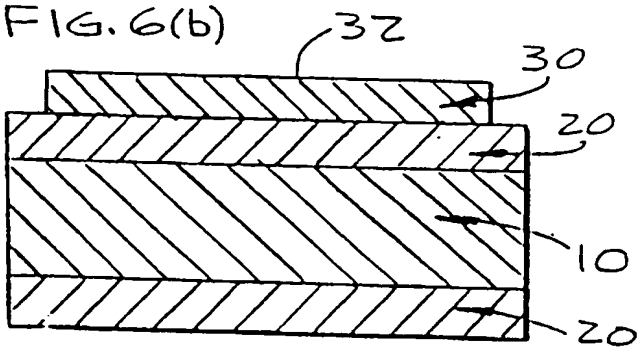


FIG.6(c)

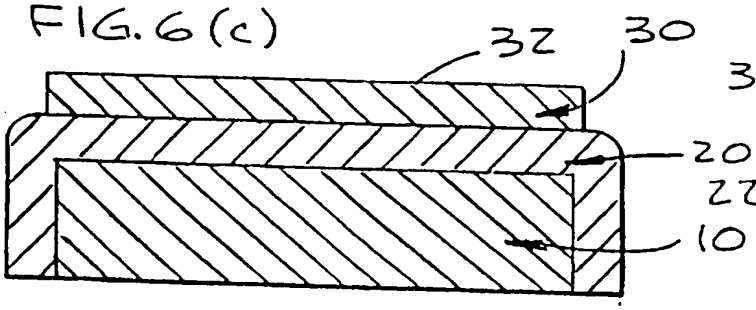


FIG.6(d)

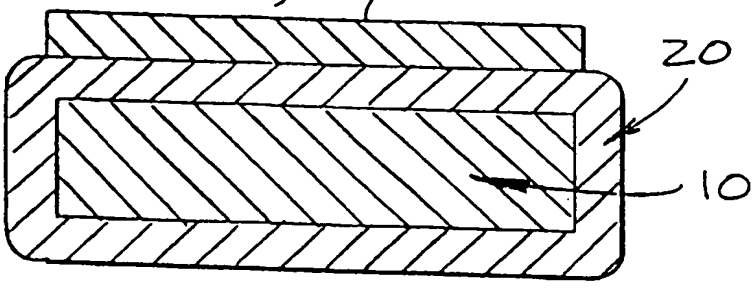


FIG.7

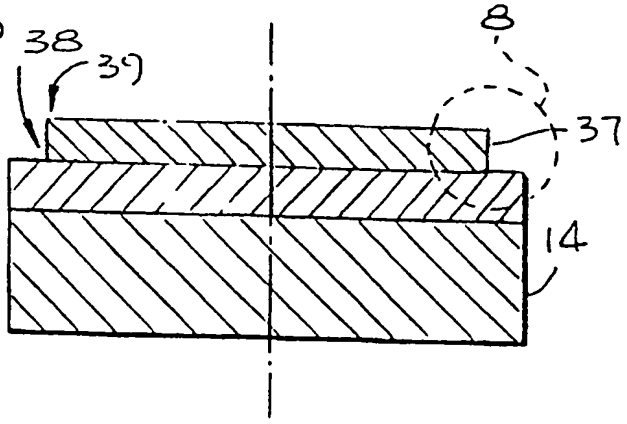


FIG.8(a)

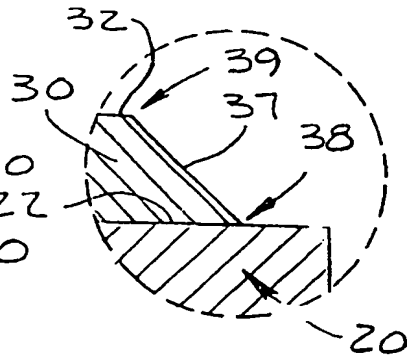
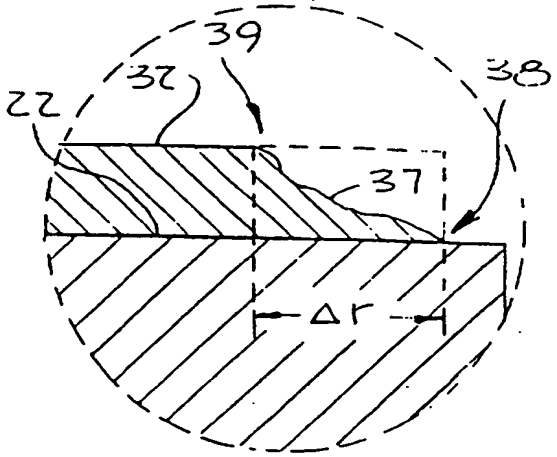


FIG. 8(b)



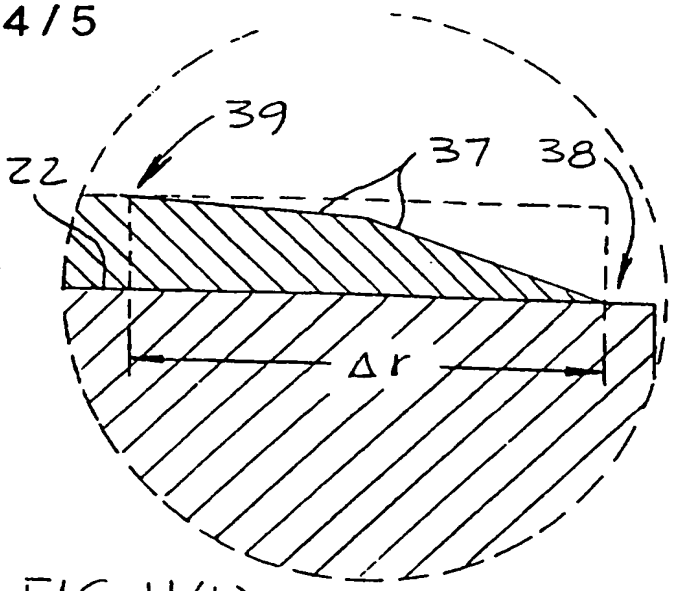
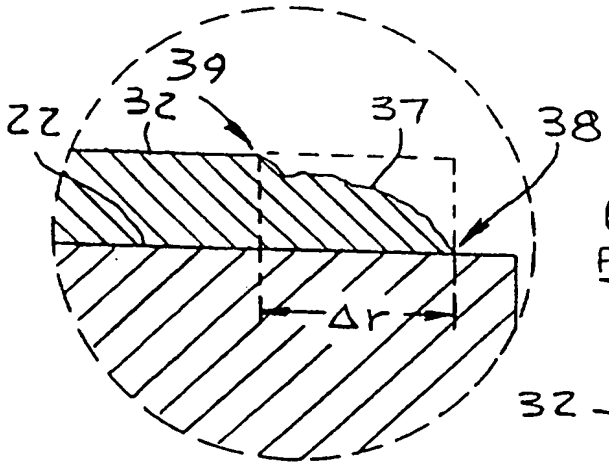


FIG. 11(b)
PRIOR ART

FIG. 8(c)



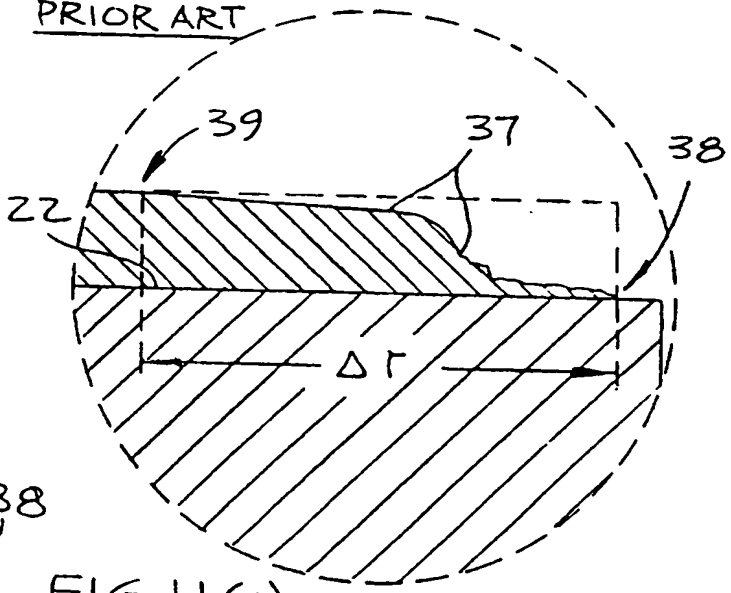


FIG. 11(c)
PRIOR ART

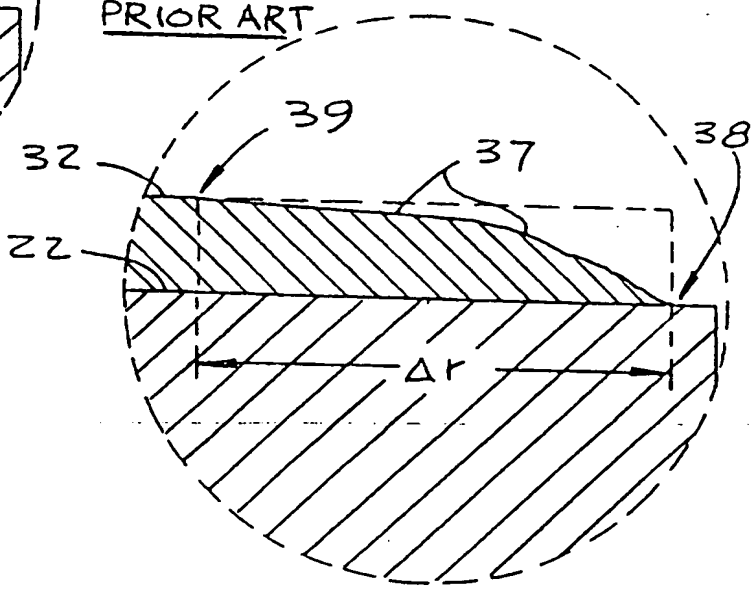


FIG. 9(a)

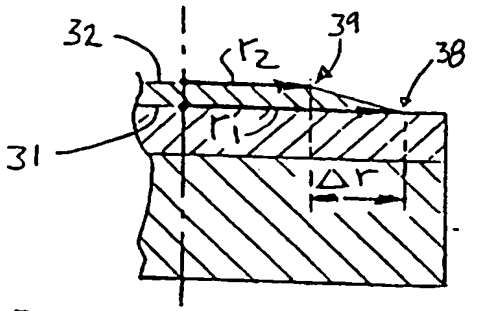


FIG. 9(b)

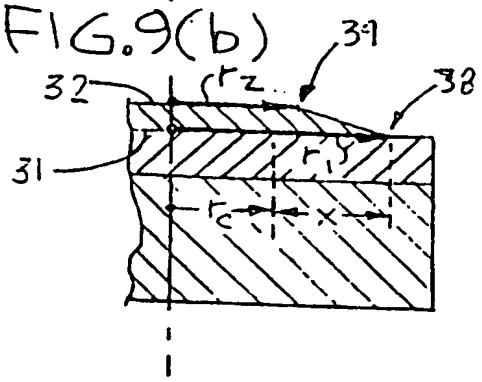
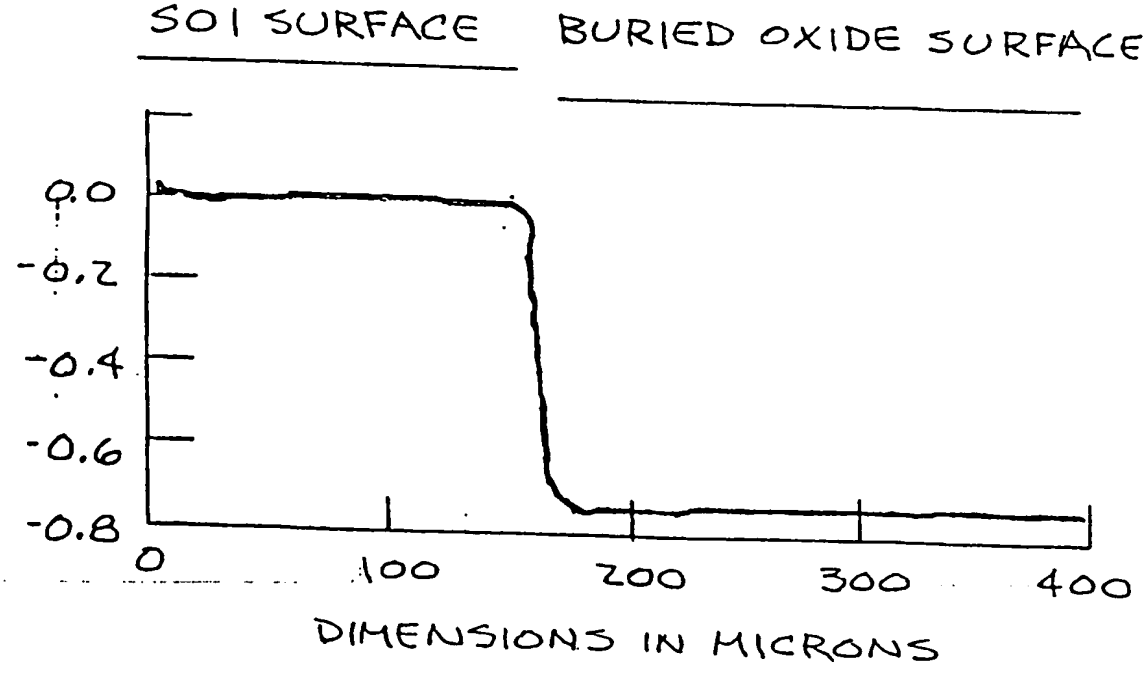


FIG. 10



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/00991

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/302, 21/3065, 21/308, 21/76, 23/13
US CL :437/62, 249; 156/632.1; 148/dig.12; 257/506, 507

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/62, 249; 156/632.1; 148/dig.12; 257/506, 507

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	US 5,340,435 A (Ito et al) 23 August 1994, col.4, lines 1-37.	21 ---- 1-20,22
Y,P	US 5,494,849 A (IYER et al) 27 February 1996, col.2, line 32-col.4, line 9	1-20,22
A	JP 7-45485 A (TOMIDA) 14 February 1995	1-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 APRIL 1997	24 JUN 1997

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	GEORGE FOURSON
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet)(July 1992)*